REMARKS

Claims 18, 27, 29-31, 33, 34, 39, 42-45 and 47 are amended, no claims are canceled, and no claims are added; as a result, claims 18-49 remain pending in this application.

Claim Objections

Applicant amends claims 27, 29-31, 33, 34, and 42 to overcome the objections as to form of the claims. Reconsideration of claims 27-34 and 42-49 is requested.

§112 Rejection of the Claims

Claim 48 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses. The subject matter of claim 48 is clearly described in the specification, for example see Fig. 1(b).

Claims 47 and 48 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses. The specification supports claims 47 and 48. For example, Fig. 1(b) shows a trench capacitor with trenches on each side. The specification at various locations describes structure and methods associated with forming buried conductors at two levels. Applicant requests withdrawal of this rejection.

§102 Rejection of the Claims

Claims 18, 19, 29, 31, 33, and 38-40 were rejected under 35 USC § 102(b) as being anticipated by Esquivel (U.S. Patent No. 4,977,439). Applicant traverses.

Applicant can not find all of the features of claim 18 in Esquivel. For example, claim 18 recites, in part, depositing a first conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, . . . depositing a second conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, . . . surrounding the first conductive material and the

second conductive material with an insulative material . . . to provide electrical insulation between the first and second conductive materials and the semiconductor substrate. As applicant can not find these features in Esquivel, applicant requests withdrawal of the rejection of claim 18 and claims 19, 29, 31, 33, and 38 which depend at least in part on claim 18.

Claim 39 recites, in part, surrounding the first conductive elements and the second conductive elements . . . to electrically insulate the first and second conductive elements from the semiconductor substrate. As applicant can not find these features in Esquivel, applicant requests withdrawal of the rejection of claim 39 and claim 40 which depends on claim 39.

§103 Rejection of the Claims

Claims 20, 27, 28, and 30 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel. Claims 20, 27, 28 and 30 all depend at least in part on claim 18 and are believed to be allowable over Esquivel for at least the reasons stated above. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Esquivel. Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Claims 21 and 24 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel, as applied to claims 18-20, 27-31, 33, and 38-40 above, and further in view of Dubin et al (U.S. Patent No. 5,891,513). Applicant respectfully traverses. Claims 21 and 24 depend from claim 18 and are believed to be allowable therewith.

Claims 21-26, 35, 36, and 41 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel, as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Gonzales (U.S. Patent No. 5,497,017). Applicant respectfully traverses. Claims 21-26, 35 and 36 depend from claim 18 and are believed to be allowable therewith. Claim 41 depends from claim 39 and is believed to be allowable therewith.

Claims 32 and 34 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel, as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Yamamoto et al. (U.S. Patent No. 5,410,169). Applicant traverses. Claims 32 and 34 depend from claim 18 and are believed to be allowable therewith.

Claim 37 was rejected under 35 USC § 103(a) as being unpatentable over Esquivel, as applied to claims 18-20, 27-31, 33, and 38-40 above, in view of Gaul (U.S. Patent No. 5,646,067). Applicant traverses. Claim 37 depends from claim 18 and is believed to be allowable therewith.

Claims 42-46 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel, in view of Gonzales. Applicant respectfully traverses. Applicant can not find all of the features of claim 18 in Esquivel. For example, claim 18 recites, in part, electrically insulating the first conductive layer from the semiconductor substrate. As applicant can not find these features in Esquivel, applicant requests withdrawal of the rejection of claim 42 and claims 43-46 which depend at least in part on claim 42.

Claim 44 was rejected under 35 USC § 103(a) as being unpatentable over Esquivel, in view of Gonzales, as applied to claims 42-46 above, and further in view of Gaul. Applicant traverses. Claim 44 depends from claim 42 and is believed to be allowable therewith.

Claims 47 and 48 were rejected under 35 USC § 103(a) as being unpatentable over Esquivel, in view of Gonzales, as applied to claims 42-46 above, and further in view of Yamamoto. Applicant traverses. Claims 47 and 48 depend at least in part from claim 42 and are believed to be allowable therewith.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 13 day of January, 2003.

Tina Kohout
Name

_____
Signature

Clean Version of Pending Claims

BURIED CONDUCTORS
Applicant: Paul A. Farrar et al.
Serial No.: 09/930,521

Claims 18-49, as of January 13, 2003 (Date of Response to Final Office Action).

18. (Amended) A method comprising:

forming at least one first trench within a semiconductor substrate at a first depth;

depositing a first conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

depositing a second conductive material, which has a melting point high enough to prevent unwanted metallurgical changes during subsequent processing, substantially at the bottom of each second trench; and

surrounding the first conductive material and the second conductive material with an insulative material to prevent short circuiting between the first conductive material and the second conductive material and to provide electrical insulation between the first and second conductive materials and the semiconductor substrate.

19. The method of claim 18, wherein the first conductive material is identical to the second conductive material.

20. The method of claim 18, wherein at least one of the first conductive material and the second conductive material comprises one of tungsten and a tungsten alloy.

21. The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, depositing a seed material to facilitate deposition of the first conductive material.

22. The method of claim 21, wherein the seed material comprises titanium.

23. The method of claim 21, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

24. The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, depositing a seed material to facilitate deposition of the second conductive material.

25. The method of claim 24, wherein the seed material comprises titanium.

26. The method of claim 24, wherein the seed material is one of an element selected from groups IVB, VB, or VIB of the periodic table.

27. (Amended) The method of claim 18, further comprising between depositing a first conductive material and forming at least one second trench, depositing the insulative material within each first trench over the first conductive material.

28. The method of claim 27, wherein the insulative material comprises silicon dioxide.

29. (Amended) The method of claim 18, further comprising after depositing a second conductive material, depositing a further insulative material within each second trench over the second conductive material.

30. (Amended) The method of claim 29, wherein the further insulative material comprises silicon dioxide.

31. (Amended) The method of claim 18, further comprising between forming at least one first trench and depositing a first conductive material, forming the insulating layer at the bottom of and on walls of each first trench.

32. The method of claim 31, wherein forming the insulating layer comprises oxidizing the bottom of and the walls of each first trench.

33. (Amended) The method of claim 18, further comprising between forming at least one second trench and depositing a second conductive material, forming a second insulating layer at the bottom of and on walls of each second trench.

34. (Amended) The method of claim 33, wherein forming the second insulating layer comprises oxidizing the bottom of and the walls of each second trench.

35. The method of claim 18, wherein at least one of the first conductive material and the second conductive material is deposited by a selective deposition process.

36. The method of claim 35, wherein the selective deposition process is selected from the group essentially consisting of chemical vapor deposition and plating.

37. The method of claim 18, wherein the semiconductor substrate is part of a wafer having a front side and a back side, and further comprising after depositing a second conductive material, thinning the back side of the wafer to expose at least one of the first conductive material and the second conductive material.

38. The method of claim 18, further comprising after depositing a second conductive material, connecting at least one of the first conductive material with at least one of the second conductive material.

39. (Amended) A method comprising:

burying first conductive elements within a semiconductor substrate at a first depth;

burying second conductive elements within a semiconductor substrate at a second depth less than the first depth; and

surrounding the first conductive elements and the second conductive elements to prevent short circuiting and to electrically insulate the first and second conductive elements from the semiconductor substrate.

40. The method of claim 39, wherein the first conductive elements and the second conductive elements each comprise a predetermined material.

41. The method of claim 39, wherein each of burying first conductive elements and burying second conductive elements comprises:

forming at least one trench within a semiconductor substrate, each trench having walls and a bottom;

forming an insulating layer at the bottom and on the walls of the trench;

depositing a seed material at the bottom of each trench;

depositing a conductive material within each trench over the seed material; and,

depositing an insulative material within each trench over the conductive material.

42. (Amended) A method, comprising:

forming communication layers in a substrate;

forming an active semiconductor layer above the communication layers on the substrate;

and

wherein forming the communication layers includes:

forming at least one first trench within a semiconductor substrate at a first depth;

forming a first insulating layer at a bottom and sidewalls of the at least one first trench;

depositing a first seed material to facilitate deposition of a first conductive material in the at least one first trench;

depositing the first conductive material substantially at the bottom of each first trench;

forming at least one second trench within the semiconductor substrate at a second depth shallower than the first depth;

forming a second insulating layer at a bottom and sidewalls of the at least one second trench;

depositing a second seed material to facilitate deposition of a second conductive material in the at least one second trench;

depositing the second conductive material substantially at the bottom of each second trench;

forming a third insulating layer on the first conductive material to prevent short circuiting to the second conductive material; and

electrically insulating the first conductive layer from the semiconductor substrate.

43. (Amended) The method of claim 42, wherein depositing the second conductive material includes forming a fourth insulating layer on the second conductive material.

44. (Amended) The method of claim 43, wherein forming the active semiconductor layer includes forming the active semiconductor layer on the fourth insulating layer.

45. (Amended) The method of claim 44, wherein forming the active semiconductor layer includes forming a P-type epitaxial layer on the fourth insulating layer.

46. The method of claim 45, wherein forming the active semiconductor layer includes forming an active circuitry of a semiconductor structure in the P-type epitaxial layer.

47. (Amended) The method of claim 46, wherein forming the active circuitry includes forming a trench capacitor that extends between the second conductive material in two of the at least one second trenches.

48. The method of claim 47, wherein forming the trench capacitor includes forming the trench capacitor with at least one first trench on opposite sides of the trench capacitor.

49. The method of claim 44, wherein forming the communication layers in the substrate includes thinning the back side of the substrate to expose at least one of the first conductive material and the second conductive material.